Specifications

* indicates programmability

*Input Voltage Ranges:	±0.5, ±1.0, ±2.0, ±5.0, ±10.0, ±20.0, ±50.0, and ±100.0 Volts (calibrated range values). A continuous ("virtual") ranging capability is provided.
*Sampling Frequencies:	0.005 Hz to 10 MHz.
*Sample Intervals:	100 ns to 200 s (internal and VXI clocks) in 100 ns steps. External clock (100 ns minimum period).
Signal Input:	
*Type:	Differential, single-ended.
Bandwidth:	dc to 5 MHz (-3 dB ±1 dB at 5 MHz).
Roll-off:	-6 dB/octave (5-10 MHz). -18 dB/octave (10-20 MHz).
*Coupling:	ac, dc, ground.
*Impedance:	50 Ohm ±1%, < 20 pF. 1 Megohm ±3%, < 20 pF. 929 Kohm ±2% < 20 pF (50V and 100V ranges).
CMRR:	> 40 dB (dc to 1 KHz) (100:1). > 50 dB (316:1) 50 Ohm typical. > 60 dB (1000:1) 1 Mohm typical.

Resolution (for twelve bits):

Range (V)	Resolution (mV/b)
±100	48.828
±50	24.414
±20.0	9.7656
±10.0	4.8828
±5.0	2.4414
±2.0	0.97656
±1.0	0.48828
±0.5	0.24414

Accuracy:

DC accuracy error (using average function):
< 0.2% of full scale ('full scale' is delta between maximum and minimum value in a range; for example, 2V in the ±1V range)
< 0.4%, ±0.5V range.
Temperature drift: <0.03% of full scale /°C (all ranges)

Dynamic Accuracy: based on least squares fit to idealized 12-bit sine wave and the formula:

Effective bits = 12 - [$\log_2$ (RMS error actual/RMS error ideal)]

Effective Bits/Typical

Range	10 KHz	100 KHz	1 MHz
0.5	> 9.36	> 9.28	> 8.14
1 V	> 9.51	> 9.44	> 8.13
2 V	> 9.00	> 8.89	> 8.15
5 V	> 9.49	> 9.01	> 7.98
10V	> 9.28	> 8.4	> 7.75
20V	> 8.6	> 7.62	--
50V	> 9.5	> 9.21	--
100V	> 28.87	> 8.42	--

Sample Memory:

Depth: 256K words (options for 512K and 1Mword).

*Control:
Pre-trigger.
Center-trigger.
Post-trigger.
Free-running.
Record mode.

*Triggering:
± External TTL-edge.
Dual ± Voltage thresholds.
Automatic (on command).
VXI TTL trigger (1 of 8 programmable).
VXI command trigger.
Any AND/OR combinations of the above.

External Trigger Uncertainty: ≤ 1 sample clock period (Trigger to first sample).

Trigger Rearm Time: 1 sample clock period (Record mode).

*Voltage Threshold Trigger Range: ±0 to ±100% full scale.

Voltage Threshold Resolution: 8 bits.

Sample Clock Accuracy: 5 ppm/yr.

External Sample Clock: TTL level, 1 50 Ohm load; dc to 10 MHz.

Delay Times:	External clock rising edge to sample delay: 30 ns ±10 ns. Sample clock to clock out delay: 12 ns ±5 ns.
*Delayed Triggering Range:	200 ns to 420 s (in 200-ns increments).
Delay Uncertainty:	≤ 200 ns (delay time). ≤ 1 sample clock (delay sample).
Gate Uncertainty:	≤ 1 sample clock (gate transition to sampling).
Data Output:	
*Formats:	ASCII. Binary. Two's-complement binary. ASCII blocks (DMA).
*Memory Control:	± offset from trigger. Auto-increment. Auto-decrement.
Processor:	
CPU:	INMOS T800 floating point transputer.
Memory:	128K bytes RAM, 128K bytes EPROM.
Embedded Preprocessor Software Routines:	Maximum value. Minimum value. Maximum value since trigger. Minimum value since trigger. Maximum positive transition. Maximum negative transition. Average value. RMS value. Ringing. Integrate. Difference. Peak-to-peak. Pulse width. Rise time. Fall time. Distortion (overshoot/undershoot). Fast Fourier Transform (FFT). Signal to noise ratio. Total harmonic distortion. Signal to noise and distortion.

Spurious free dynamic range.
Mean/standard deviation.
Period.
Frequency.
Duty cycle.

I/O Connections:

2 - BNC Jacks.
1 - DB25 25 pin connector.

Inputs:

TRIG IN, one TTL load, programmable to positive or negative edge true.

CLK IN, 50 Ohm load.
Clock high time minimum: 50 ns.
Clock low time minimum: 50 ns.

ARM IN, one TTL load programmable to positive or negative edge true.

GATE, one TTL load, active low.
Gate high time minimum: 50 ns.
Gate low time minimum: 50 ns.

SIG IN + (BNC): CAT II, 150 V DC, 120 V AC, into 1 M Ohm
10 V DC, 50 Ohms

SIG IN – (BNC): CAT II, 150 V DC, 120 V AC, into 1 M Ohm
10 V DC, 50 Ohms

Outputs (TTL):

CLK OUT, TTL, 50% duty cycle, 50 Ohm line driver.

TRIG OUT, TTL, programmable to active low or high (trigger detection).

ARM OUT, TTL, programmable to active low or high.

Self Test:

The module automatically performs a self test on power-up. The test consists of verifying the CPU and data memory, module's internal buses, and analog input circuitry. Self test may also be performed on command.

VXIbus Compatibility:

Fully compatible with the VXIbus Specification V1.4 for message-based instruments with the Halt switch in the ON position.

VXI Device Type:

VXI message based instrument.

VXI Protocol:

Word serial.

Dynamic Configuration:	Yes (set LA switch to FFh).
VXI Card Size:	C size, one slot wide.
Module-Specific Commands:	All module-specific commands and data are sent via the VXIbus Byte Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.
VMEbus Interface:	Data transfer bus (DTB) slave - A16, D16 only.
Interrupt Level:	Switch selectable, levels 1 (highest priority) through 7 (lowest); or programmable.
Interrupt Acknowledge:	D16; lower 8 bits returned are the logical address of the module.
VXIbus Commands Supported:	All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command error: ABORT NORMAL OPERATION ASSIGN INTERRUPT LINE ASYNCHRONOUS MODE CONTROL BEGIN NORMAL OPERATION BYTE AVAILABLE (with or without END bit set) BYTE REQUEST CLEAR CLEAR LOCK CONTROL EVENT END NORMAL OPERATION ERROR QUERY READ INTERRUPT LINE READ INTERRUPTER READ PROTOCOL READ STATUS SET LOCK TRIGGER
VXIbus Protocol Events Supported:	VXIbus events are returned via VME interrupts. The following event is supported and returned to the module's commander: REQUEST TRUE (In IEEE-488 systems, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)

VXIbus Registers:	ID Device Type Status Control Protocol Response Data Low See Appendix A for definition of register contents.
Device Type Register Contents:	FDF7
Power Requirements:	All required dc power is provided by the Power Supply in the VXIbus mainframe.
Voltage:	+5 Volt Supply: 4.75 V dc to 5.25 V dc. -2 Volt Supply: -1.9V dc to -2.1 V dc. +24 Volt Supply: +23.5 V dc to +24.5 V dc. -24 Volt Supply: -23.5 V dc to -24.5 V dc.
Current (Peak Module, I_{PM}):	+5 Volt supply: 3.85A -5.2 Volt Supply: 0.6A -2.0 Volt Supply: 0.026 A +24 Volt Supply: 0.22 A -24 Volt Supply: 0.23 A
Fuses:	Replacement fuses: **Littelfuse** P/N 273005 (5 amp) and 273002 (2 amp) **125 V VFBIo (very fast blow).**
Cooling:	Provided by the fan in the VXIbus mainframe. Less than 10°C temperature rise with 2.7 liters/sec of air at a pressure drop of 0.19 mm of H_2O.
Temperature:	-10°C to +65°C, operating (assumes ambient temperature of 55° and airflow to assure less than 10°C temperature rise). -40°C to +85°C, storage.
Humidity:	Less than 95% R.H. non-condensing, -10°C to +30°C. Less than 75% R.H. non-condensing, +31°C to +40°C. Less than 45% R.H. non-condensing, +41°C to +55°C.
Radiated Emissions:	Complies with VXIbus Specification.
Conducted Emissions:	Complies with VXIbus Specification.
Module Envelope Dimensions:	197 mm high, 221 mm deep, 13 mm wide. (7.75 in x 8.69 in x 0.5 in).

Dimensions, Shipping:	When ordered with a Tek/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, the module's shipping dimensions are: 254 mm x 254 mm x 127 mm. (10 in x 10 in x 5 in).
Weight:	Fully configured, with Option 02 and Option 03: 1.6 kg. (3 lb 8.4 oz.)
Weight, Shipping:	When ordered with a Tek/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1-12). When ordered alone, the module's shipping weight is: 2.1 kg. (4 lb 8.4 oz.)
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connectors:	2 BNC inputs, 1 DB25S connector. Refer to Appendix B for connector pinouts.
Equipment Supplied:	1 - VX4240 Waveform Digitizer/Analyzer Module. 1 - Spare fuse +5V 1 - Spare Fuse, ±24V, -2V, -5.2V
Optional Equipment:	1 - 73A-742P 5-meter, 25 pin cable, unterminated.
Options:	01 512K memory. 02 1 Meg memory. 03 Digital Signal Processor.

Conditions for Safety Certification:

Operating Temperature:	**+5 to +40 °C**
Maximum Operating Altitude:	**2000 m**
Equipment Type:	**Test and measuring**
Safety Class:	**Class I (as defined in in IEC1010-1, Annex H) grounded product.**
Overvoltage Category:	**Supply Input:** **Overvoltage Category I (as defined in IEC1010-1, Annex J).** **Measuring Inputs:** **Overvoltage Category II (as defined in IEC1010-1, Annex J).**
Pollution Degree:	**Pollution Degree 2 (as defined in IEC1010-1). Rated for indoor use only.**